invention taken along section line A-A' in Figure 32.

Figure 34 is a sectional view through a typical EEPROM cell according to the teachings of the invention taken along section line B-B' in Figure 32.

DETAILED DESCRIPTION OF THE [INVENTION] PREFERRED EMBODIMENT

Referring to Figure 1, there is shown a cross-sectional view of an intermediate stage in the construction of the EEPROM memory cell according to the teachings of the invention. Although a detailed process schedule and series of drawings illustrating the exact method of making one embodiment of the invention will be presented below, Figures 1-3 will be used to summarize the construction of an EEPROM memory cell according to the teachings of the invention.

To reach the stage of construction shown in Figure 1, a one micron deep well is etched into an N type silicon substrate 10 having a resistivity of 10 Ohm centimeter. A P doped region 12 is formed about midway down the well. An N doped region 14 lies above the P type region 12. An oxide layer 16 having a thickness of about 2000 angstroms is grown on top of the substrate. An oxide layer 18 is grown at the bottom of the well and has a thickness of about 1000 angstroms. A thin annular oxide layer, sections of which are shown at 20 and 20', is grown on the sidewalls of the well to insulate a first layer of doped polysilicon 22 which is deposited on the surface of the substrate and into the well.

Figure 2 shows a subsequent stage of construction after an anisotropic etchback to remove the upper portions of the first polysilicon layer and the first polysilicon lying in the bottom of the well above oxide layer 18. This leaves a floating gate comprised of an annular first polysilicon layer, two sections of which are shown at 22 and 22'. This floating gate is isolated from the substrate by the thin oxide layer 20. To complete the electrical isolation of the floating gate layer 22, a layer of ONO insulator 24 is deposited over the surface of the substrate and in the well.

The thickness and integrity of the ONO layer is important to the coupling ratio in an EEPROM which is important in the write process. Referring to Figure 3, there is shown an equivalent circuit of the floating gate and control gate structure shown in Figure 4. Although Figure 4 represents the structure of a typical prior art floating gate EEPROM structure, it is used here to illustrate the functioning of an EEPROM cell and the significance to the write process of the coupling ratio